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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,397	04/14/2005	Franciscus Johannes Klosters	NL02 1018 US	6217

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EXAMINER	
FLORES, LEON	

ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
07/22/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/531,397	KLOSTERS ET AL.	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) *2* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1, 3-7) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that, *"the combination of Sato and Pohlmeyer does not teach suppressing the supply of sampling clock signals after an end of a preceding message until a condition for supplying of sampling clock signals is met, as recited in the claim".*

The examiner respectfully disagrees. The reference of Sato does suggest suppressing the supply of sampling clock signals after an end of a preceding message until a condition for supplying of sampling clock signals is met. (See figs 7 & 10: 53, 55, 57, 59, 61, 63, 65 & col. 8, line 23 - col. 9, line 67 "the supply of the sampling clock signals depend on the detection of the synchronization patterns")

Applicant further asserts that, *"Pohlymeyer does not teach verifying that the duration of one or more internal intervals correspond to a specified bit period. Additionally, the Office Action does not assert that Sato might teach the missing limitation of Pohlmeyer. Accordingly, Applicants respectfully assert that claim 4 is patentable over Sato and Pohlmeyer because Pohlmeyer does not teach "to verify whether one or more internal intervals between communication signal level changes in said sync field interval have durations corresponding to the bit period specified by the sync field interval as a further condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval," as recited in claim 4".*

The examiner agrees. However, a new ground of rejection has been issued.

Applicant finally asserts that, *"claim 6 is patentable over the combination of Sato and Pohlmeyer because the combination of cited references does not teach all of the limitations of the claim. Claim 6 recites "a comparison circuit for comparing each time a combination of the first and a second number of a respective one of the potential sync break intervals and the sync field interval identified therewith, the comparison circuit outputting an enabling signal to enable supplying the sampling clock signal at the adapted frequency when a ratio between the first and second number in a combination is in a predetermined range" (emphasis added)".*

The examiner respectfully disagrees. The reference of Sato does suggest a comparison circuit for comparing each time a combination of the first and a second number of a respective one of the potential sync break intervals and the sync field interval identified therewith, the comparison circuit outputting an enabling signal to enable supplying the sampling clock signal at the adapted frequency when a ratio between the first and second number in a combination is in a predetermined range. (See col. 9, line 51 – col. 10, line 1 "the interval detector measures the time interval of the maxima in terms of sampling clocks as a detected count of the sampling clocks" "the frame period is known as a reference count of the sampling clocks" "it compares the measured count with the reference count")

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims (1-7) are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 1 recites the limitation "sampling clock signals" in line 18. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 7 recites the limitation "sampling clock signals" in line 14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. **Claims (1 & 3-7) are rejected under 35 U.S.C. 103(a) as being unpatentable over Pohlmeyer et al. (hereinafter Pohlmeyer) (US 2002/0101884 A1) in view of Sato et al. (hereinafter Sato) (US Patent 5,596,582)**

Re claim 1, Pohlmeyer discloses a data processing apparatus, for receiving a communication signal that comprises a message containing a sync break interval with a unique bit pattern, the message containing a sync field interval identified by the sync break interval, a timing property of the sync field interval specifying a length of bit periods of the message, the apparatus comprising: an input port for receiving the communication signal (See fig. 1 & ¶ 16); a reception circuit for sampling and processing bits from the message. (See fig. 1 & ¶ 16)

But the reference of Pohlmeyer fails to teach a clock source circuit for supplying a sampling clock signal to the reception circuit to define time points for said sampling, the clock source circuit being arranged to adapt a frequency of the sampling clock signal to the timing property of the sync field interval, the clock source circuit being arranged to search for potential sync break intervals that match the unique bit pattern for a range of bit period values, the clock source circuit verifying for each potential sync break interval whether the sync field interval identified by that potential sync break interval specifies a bit period with a duration so that the sync break interval matches the unique pattern for the specified bit period, as a condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval identified by the

potential sync break interval.

However, Sato does. (See figs 7 & 10: 53, 55, 57, 59, 61, 63, 65 & col. 8, line 23 - col. 9, line 67) Sato discloses a clock source circuit for supplying a sampling clock signal to the reception circuit to define time points for said sampling, the clock source circuit being arranged to adapt a frequency of the sampling clock signal to the timing property of the sync field interval, the clock source circuit being arranged to search for potential sync break intervals that match the unique bit pattern for a range of bit period values, the clock source circuit verifying for each potential sync break interval whether the sync field interval identified by that potential sync break interval specifies a bit period with a duration so that the sync break interval matches the unique pattern for the specified bit period, as a condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval identified by the potential sync break interval.

Therefore, taking the combined teachings of Pohlmeyer and Sato as a whole, it would have been obvious to one of ordinary skills in the art to have incorporated these features into the system of Sato, in the manner as claimed and as taught by Pohlmeyer, for the benefit of generating optimum sampling clock signals based on detecting the synchronization patterns.

The combination of Pohlmeyer and Sato discloses the limitations as claimed above, except they fail to explicitly teach that wherein supply of sampling clock signals is suppressed after an end of a preceding message until said condition is met.

However, the reference of Sato does suggest (See figs 7 & 10: 53, 55, 57, 59,

61, 63, 65 & col. 8, line 23 - col. 9, line 67) that wherein supply of sampling clock signals is suppressed after an end of a preceding message until said condition is met. ("the supply of the sampling clock signals depend on the detection of the synchronization patterns")

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated these features into the system of Pohlmeyer, as modified by Sato, in the manner as claimed, for the benefit of generating optimum sampling clock signals based on detecting the synchronization patterns.

Re claim 3, the combination of Pohlmeyer & Sato further teaches that wherein said unique pattern contains a repetition of a same bit value for more than a maximum number of bit periods during which the same bit value is permitted to be repeated during a remainder of the message. (In Pohlmeyer, see figs 3 & 4 & ¶ 21)

Re claim 4, the combination of Pohlmeyer & Sato fails to explicitly teach that fails to explicitly teach that wherein the clock source circuit is arranged furthermore to verify whether one or more internal intervals between communication signal level changes in said sync field interval have durations corresponding to the bit period specified by the sync field interval as a further condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval.

However, the reference of Sato does suggest (See figs 7 & 10: 59 & col. 9, lines 51-62) that wherein the clock source circuit is arranged furthermore to verify whether

one or more internal intervals between communication signal level changes in said sync field interval have durations corresponding to the bit period specified by the sync field interval ("the interval detector measures a time interval F between two maxima" "when the maxima is substantially coincident with the frame period, synchronization patterns have been detected") as a further condition prior to supplying the sampling clock signal at the adapted frequency specified by the sync field interval. ("synchronization patterns are used to make the frequency converter control the controllable oscillator")

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated these features into the system of Pohlmeyer, as modified by Sato, in the manner as claimed, for the benefit of detecting the synchronization pattern and controlling the oscillator.

Re claim 5, the combination of Pohlmeyer & Sato further discloses that wherein the clock source circuit operates in parallel with the reception circuit, proceeding with said searching while said reception circuit is sampling bits from the communication signal. (In Sato, see fig. 7: 51 & 65 & col. 8, lines 23-50, 59-65)

Re claim 6, the combination of Pohlmeyer & Sato further teach that wherein the clock source circuit comprises a local clock circuit for generating a local clock signal. (In Sato, see fig. 7: 65)

But the combination of Pohlmeyer & Sato fails to explicitly teach that counter means for counting respective first numbers of periods of said local clock signal that

occur in the potential sync break intervals and respective second numbers of periods of the local clock signal that characterize the timing property of the sync field intervals identified by the potential sync break intervals and a comparison circuit for comparing each time a combination of the first and a second number of a respective one of the potential sync break intervals and the sync field interval identified therewith, the comparison circuit outputting an enabling signal to enable supplying the sampling clock signal at the adapted frequency when a ratio between the first and second number in a combination is in a predetermined range.

However, the reference of Sato does suggest (See col. 9, line 51 – col. 10, line 1) that counter means for counting respective first numbers of periods of said local clock signal that occur in the potential sync break intervals and respective second numbers of periods of the local clock signal that characterize the timing property of the sync field intervals identified by the potential sync break intervals and a comparison circuit for comparing each time a combination of the first and a second number of a respective one of the potential sync break intervals and the sync field interval identified therewith, the comparison circuit outputting an enabling signal to enable supplying the sampling clock signal at the adapted frequency when a ratio between the first and second number in a combination is in a predetermined range. (“the interval detector measures the time interval of the maxima in terms of sampling clocks as a detected count of the sampling clocks” “the frame period is known as a reference count of the sampling clocks” “it compares the measured count with the reference count")

Therefore, it would have been obvious to one of ordinary skills in the art to have incorporated these features into the system of Pohlmeyer, as modified by Sato, in the manner as claimed, for the benefit of detecting the synchronization pattern and controlling the oscillator.

Claim 7 is a method claim corresponding to system claim 1. Hence, the steps performed in method claim 7 would have necessitated the elements in system claim 1. Therefore, claim 7 has been analyzed and rejected w/r to claim 1 above.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. F./
Examiner, Art Unit 2611
July 11, 2008

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611